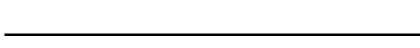
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# DATA SHEET



# MOS FIELD EFFECT TRANSISTOR NP100P04PLG

# SWITCHING **P-CHANNEL POWER MOSFET**

#### **DESCRIPTION**

The NP100P04PLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

#### <R> ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
NP100P04PLG-E1-AY Note		Tara 000 alasal	TO 000 (MD 057D)	
NP100P04PLG-E2-AY Note	Pure Sn (Tin)	Tape 800 p/reel	TO-263 (MP-25ZP)	

Note Pb-free (This product does not contain Pb in external electrode.)

#### **FEATURES**

• Super low on-state resistance

 $R_{DS(on)1}$  = 3.7  $m\Omega$  MAX. (Vgs = -10 V, Ip = -50 A)

 $R_{DS(on)2} = 5.1 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = -4.5 \text{ V, Ip} = -50 \text{ A)}$ 

• High current rating: I<sub>D(DC)</sub> = ∓100 A

· Built-in gate protection diode

# (TO-263)



## ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (VGS = 0 V)	VDSS	-40	V
Gate to Source Voltage (Vps = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	I <sub>D(DC)</sub>	∓100	Α
Drain Current (pulse) Note1	D(pulse)	∓300	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	200	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note2	las	74	Α
Single Avalanche Energy Note2	Eas	550	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = -20  $\rightarrow$  0 V

## THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	0.75	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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# **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

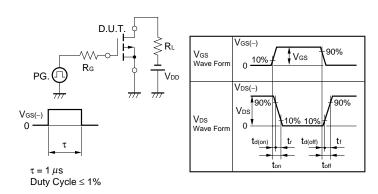
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V			-10	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ∓20 V, V <sub>DS</sub> = 0 V			∓10	μΑ
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	<b>y</b> fs	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -50 A	43	88		S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -50 A		2.8	3.7	mΩ
	RDS(on)2	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -50 A		3.4	5.1	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = -10 V,		15100		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		2400		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		1130		pF
Turn-on Delay Time	t <sub>d(on)</sub>	$V_{DD} = -20 \text{ V}, I_D = -50 \text{ A},$		38		ns
Rise Time	tr	V <sub>GS</sub> = -10 V,		30		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		300		ns
Fall Time	<b>t</b> f			100		ns
Total Gate Charge	Q <sub>G</sub>	$V_{DD} = -32 \text{ V},$		320		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = -10 V,		37		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -100 A		85		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = -100 A, V <sub>GS</sub> = 0 V		0.91	1.5	V
Reverse Recovery Time	trr	I <sub>F</sub> = -100 A, V <sub>GS</sub> = 0 V,		70		ns
Reverse Recovery Charge	Qrr	di/dt = –100 A/μs		123		nC

**Note** Pulsed test PW  $\leq$  350  $\mu$ s, Duty Cycle  $\leq$  2%

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

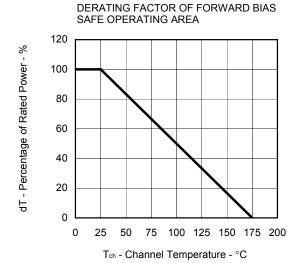
# $V_{GS} = -20 \rightarrow 0 \text{ V}$ $V_{DD}$ $V_{DD}$

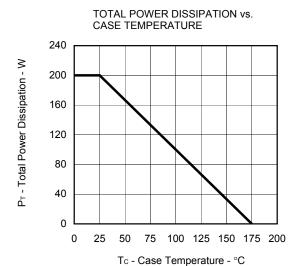
# TEST CIRCUIT 2 SWITCHING TIME



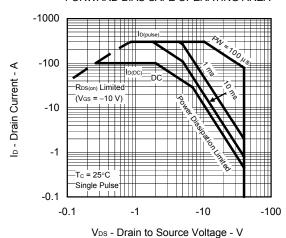
# **TEST CIRCUIT 3 GATE CHARGE**

# TYPICAL CHARACTERISTICS (TA = 25°C)

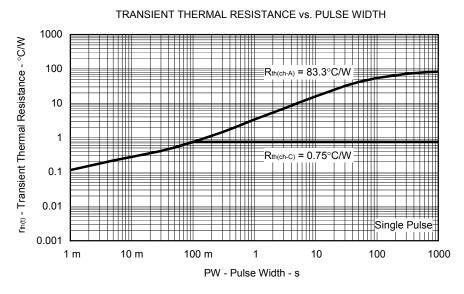




#### FORWARD BIAS SAFE OPERATING AREA

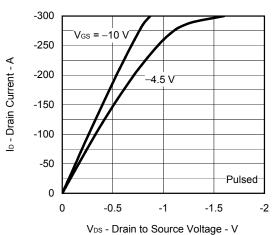


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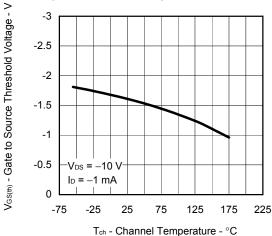


3

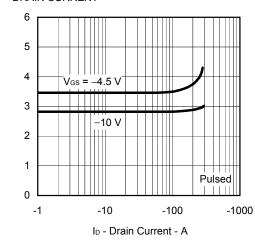




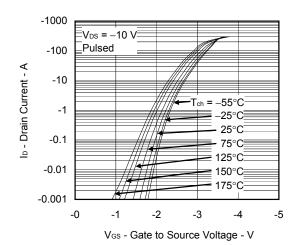
#### GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



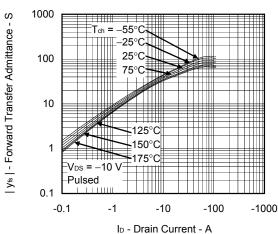
#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



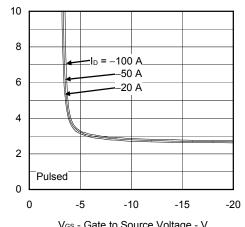
#### FORWARD TRANSFER CHARACTERISTICS



#### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



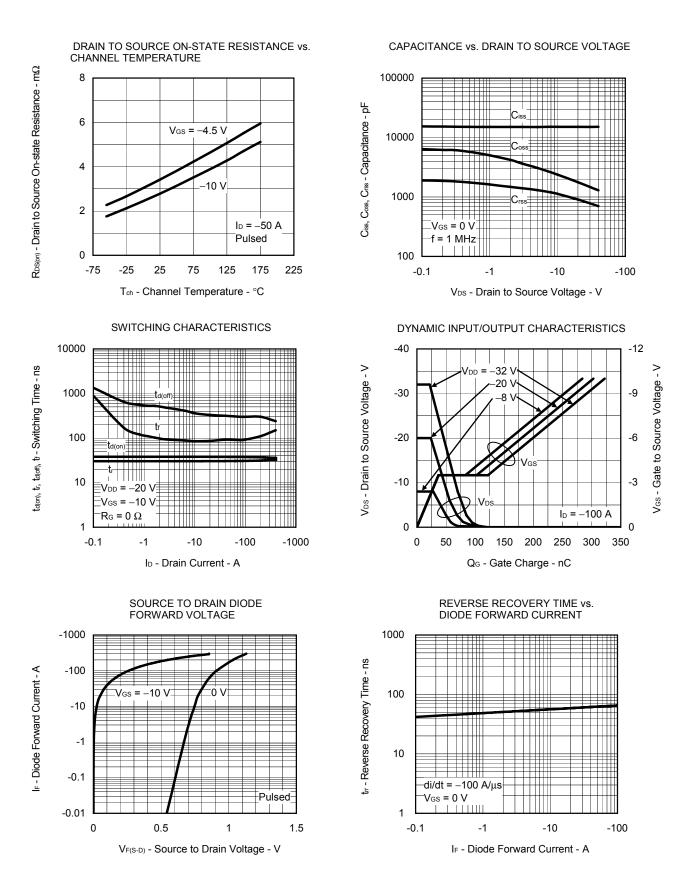
#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



V<sub>GS</sub> - Gate to Source Voltage - V

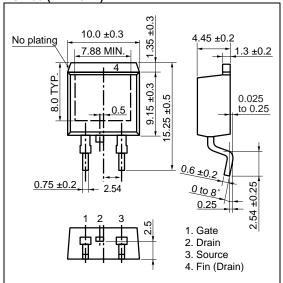
R<sub>DS(o1)</sub> - Drain to Source On-state Resistance - mΩ

RDS(on) - Drain to Source On-state Resistance - mΩ

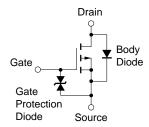


# PACKAGE DRAWING (Unit: mm)

# TO-263 (MP-25ZP)



# **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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